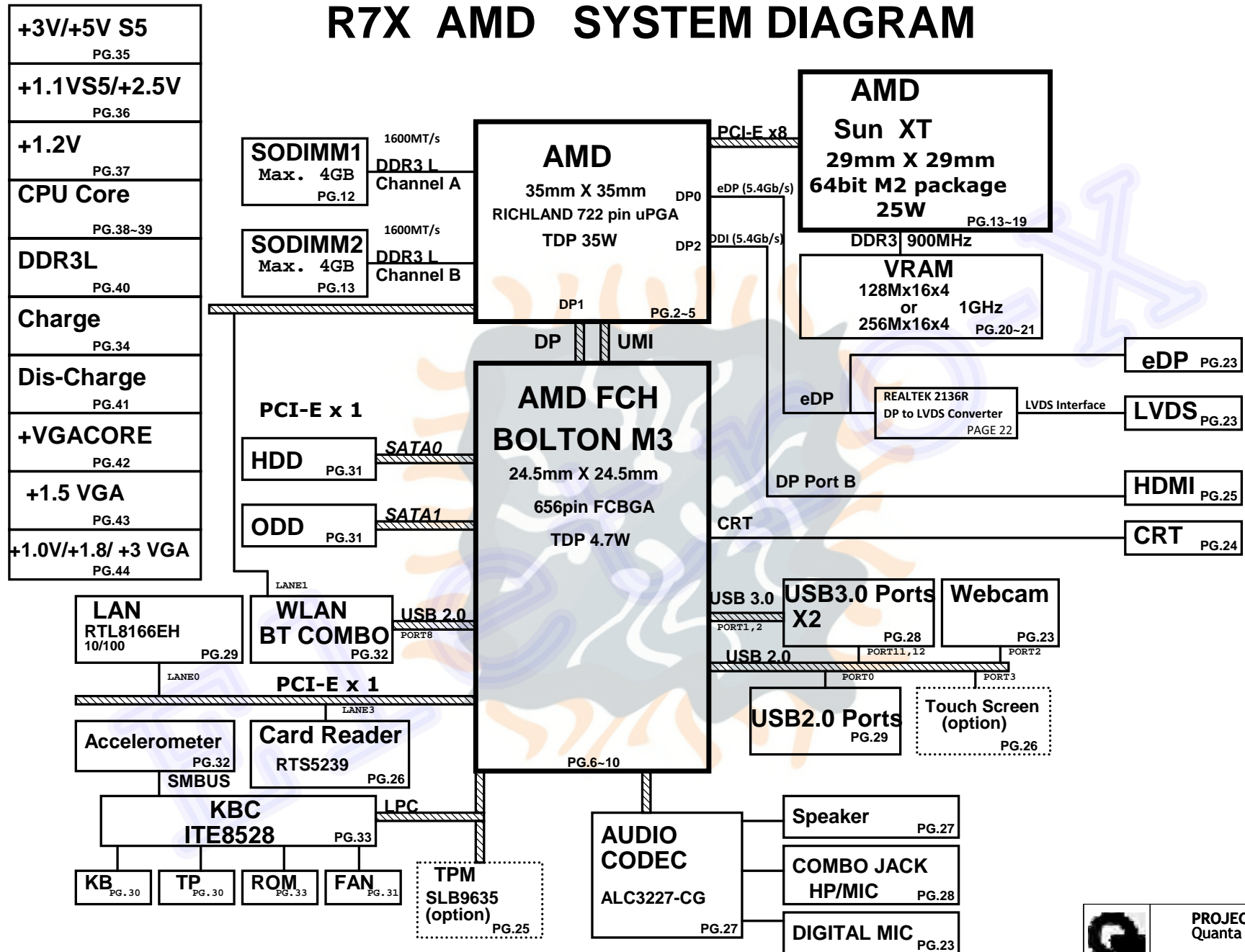
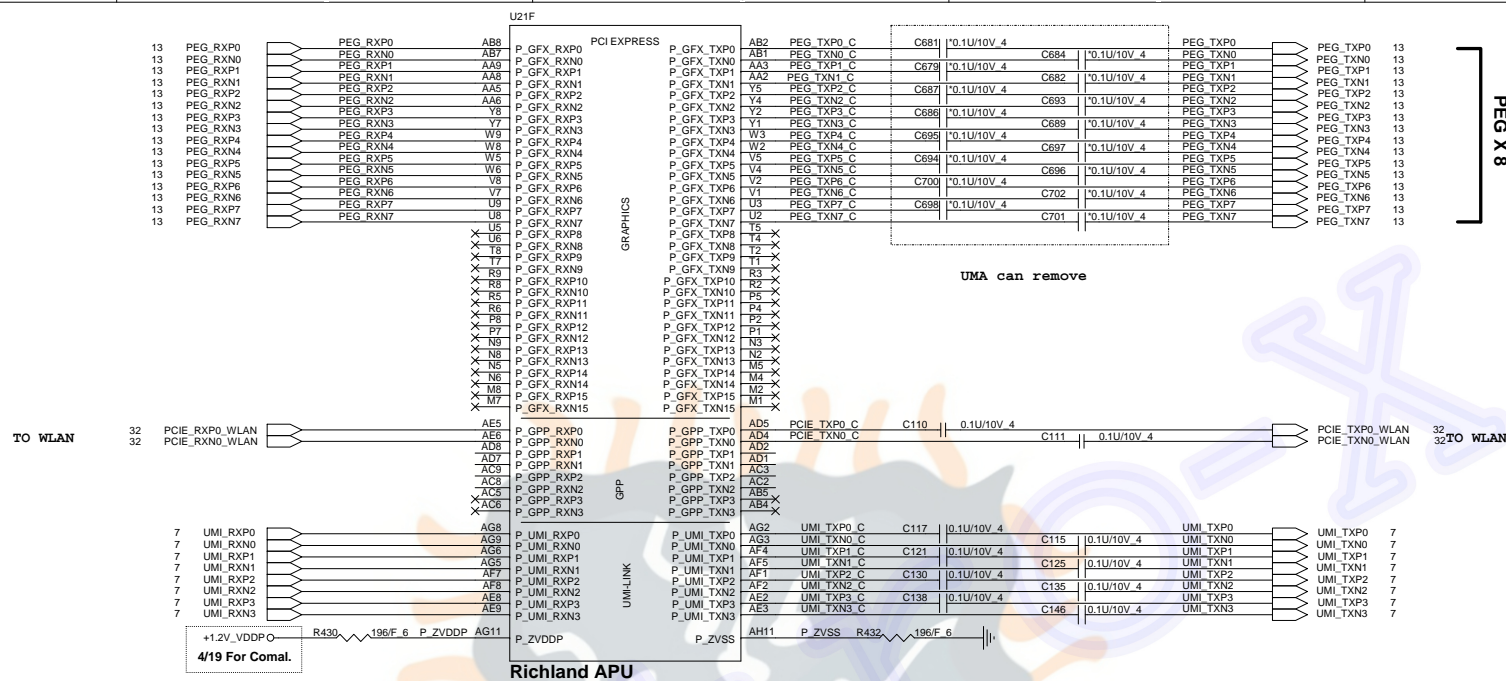


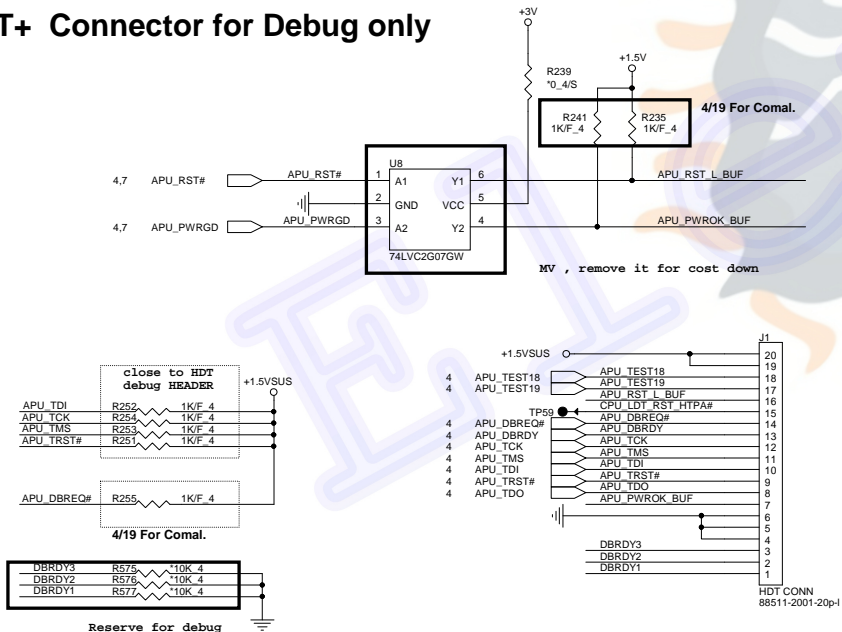
R7X AMD SYSTEM DIAGRAM

01

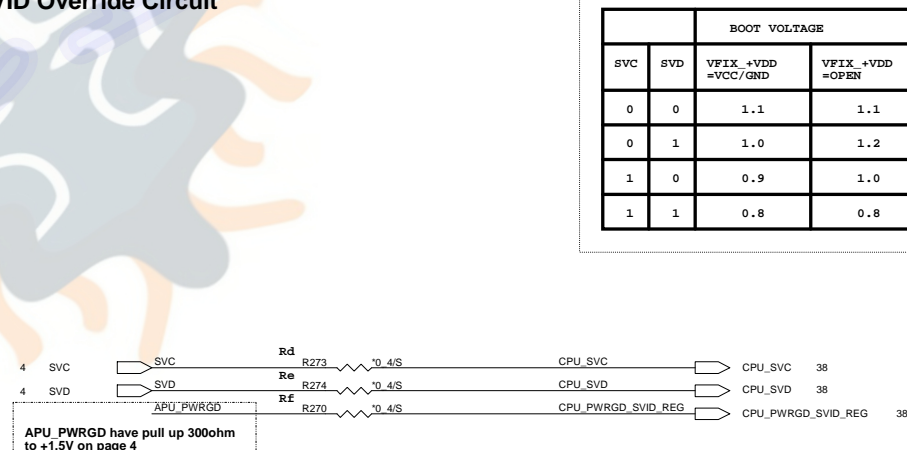




HDT+ Connector for Debug only



VID Override Circuit

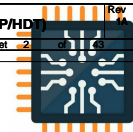


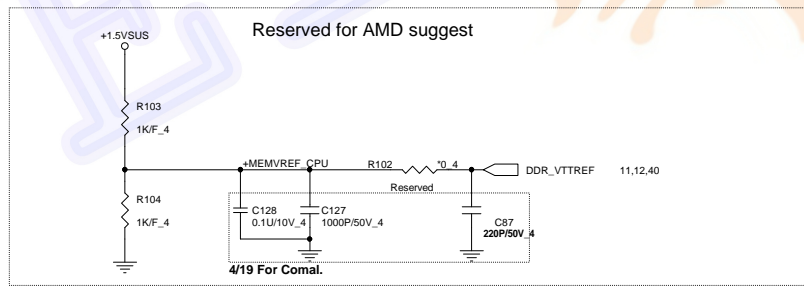
		BOOT VOLTAGE	
SVC	SVD	VFIX +VDD =VCC/GND	VFIX +VDD =OPEN
0	0	1.1	1.1
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8



PROJECT : R7X
Quanta Computer Inc.

Size Custom	Document Number APU 1/4(PCIE/UMI/GPP/HD
Date: Tuesday, March 12, 2013	Sheet 2

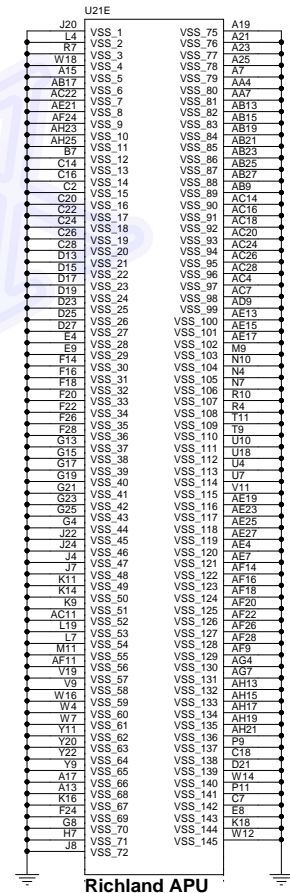
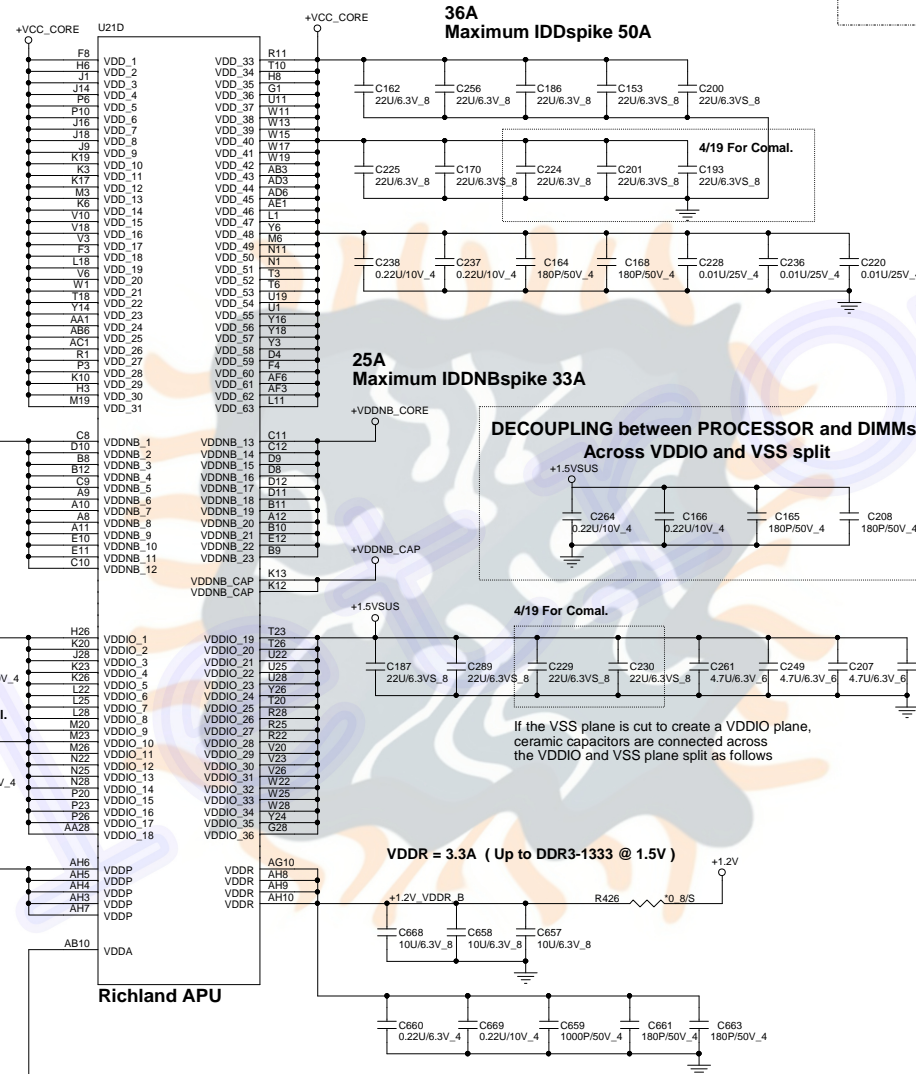
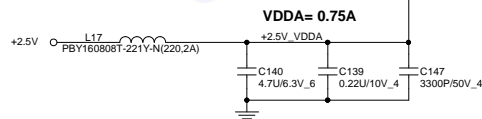
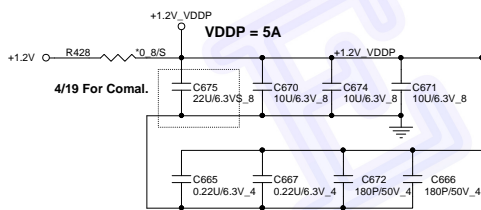
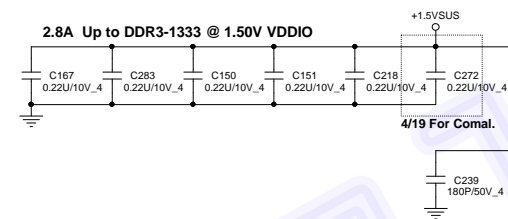
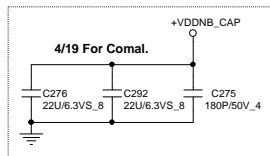
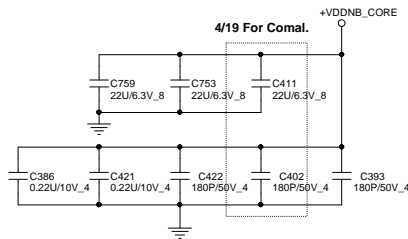
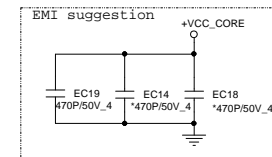




Size Custom	Document Number APU 2/4(DDR3 MEM I/F)
Date: Tuesday, March 12, 2013	Sheet

APU POWER TABLE

PIN NAME	NET NAME	VOLTAGE
VDD	+VCC_CORE	+1.1V
VDDNB	+VDDNB_CORE	??
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V



Richland APU

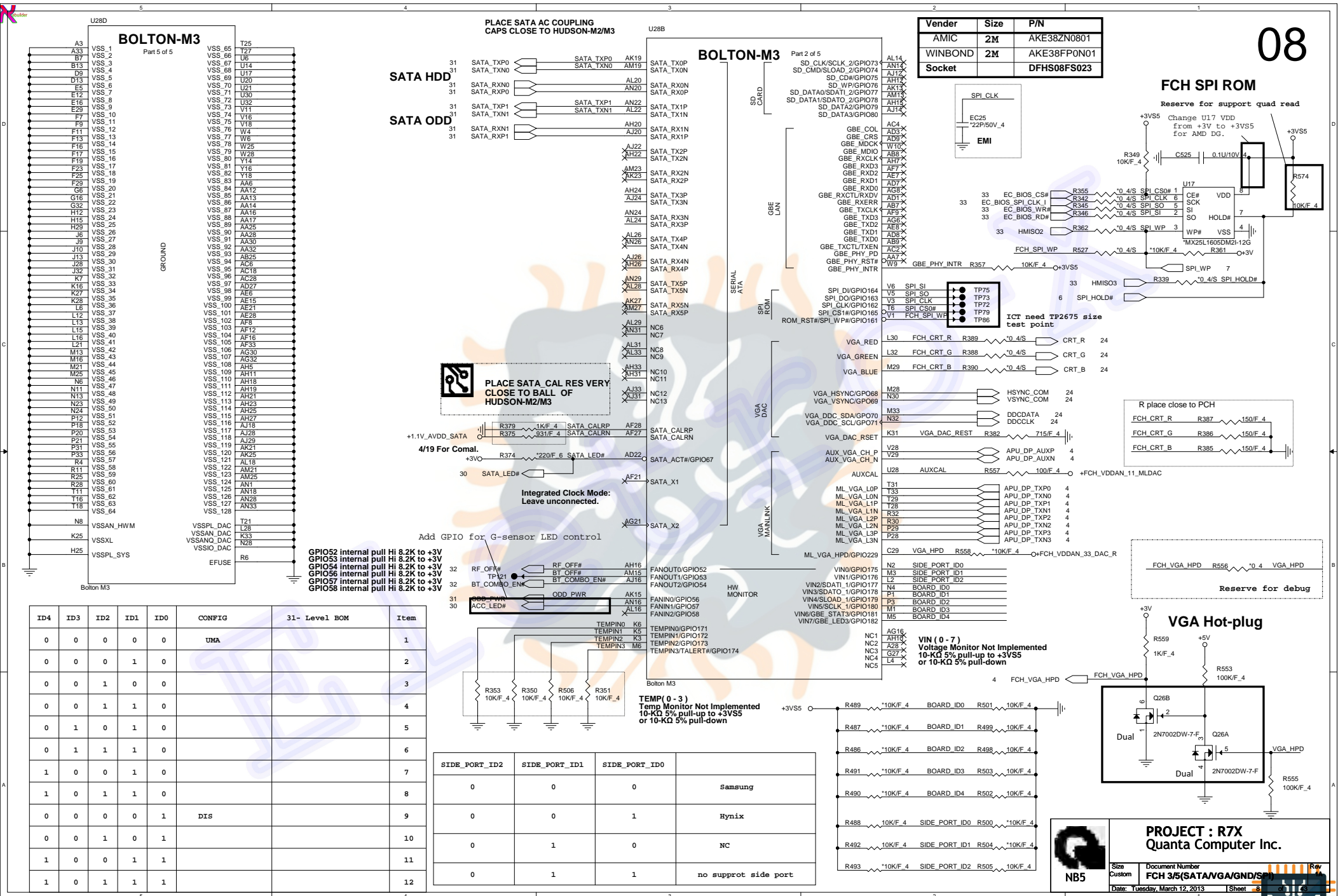


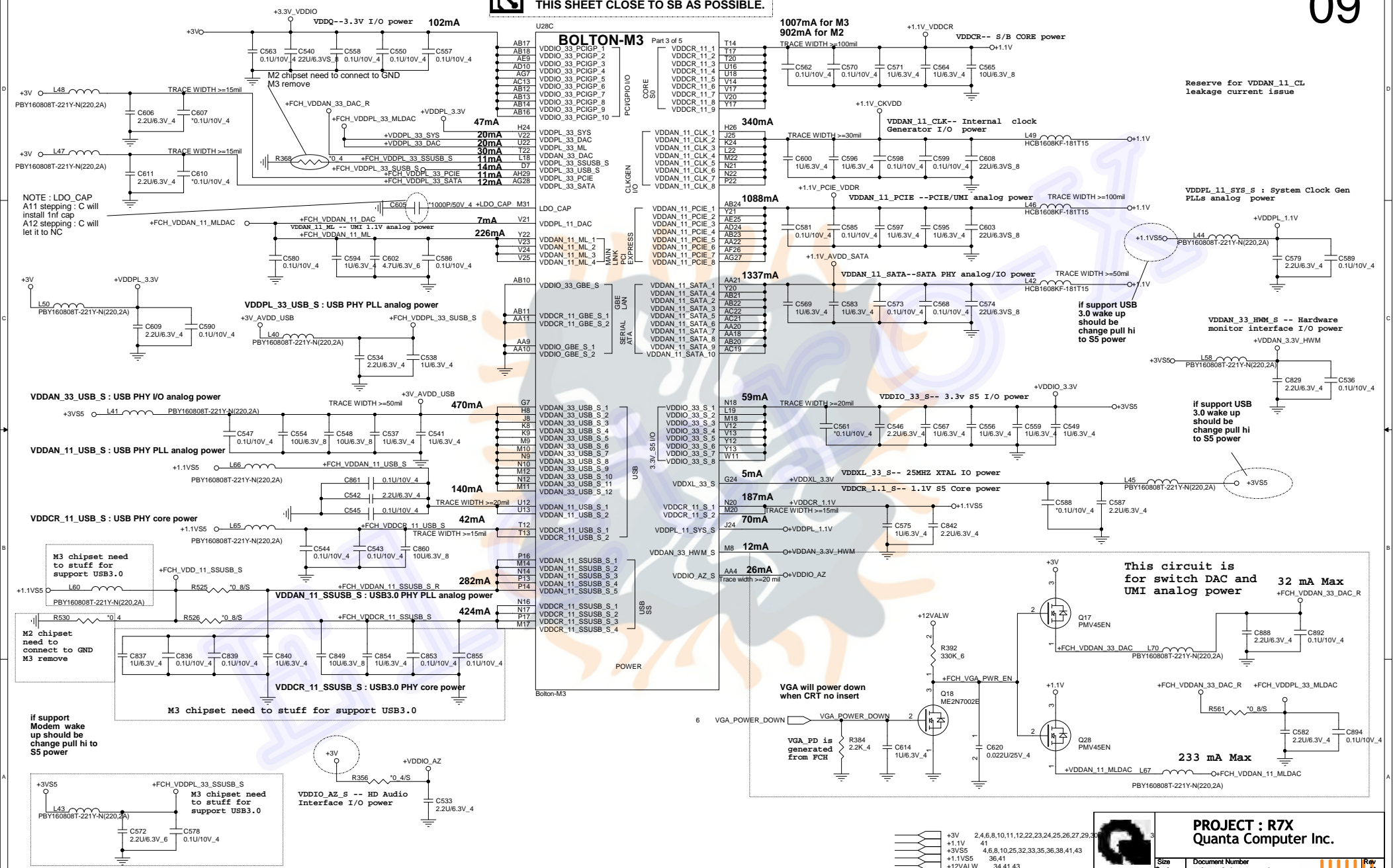
PROJECT : R7X
Quanta Computer Inc.

Size Custom Document Number
APU 4/4(Power/GND)
Date: Tuesday, March 12, 2013 Sheet 5





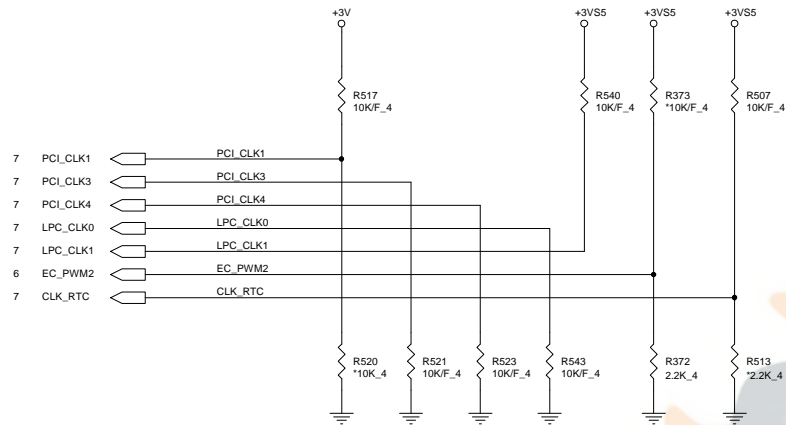




STRAPS PINS



OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

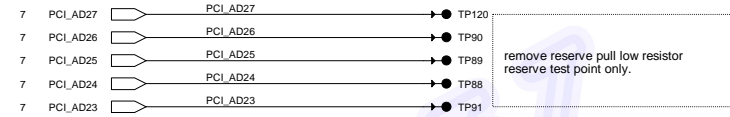


REQUIRED STRAPS

	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	CLK_RTC
PULL HIGH	ALLOW PCIe Gen2 DEFAULT	USE DEBUG STRAP	non Fusion CLOCK MODE	AMD internal EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIe Gen1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	SPI ROM	S5 PLUS MODE ENABLED

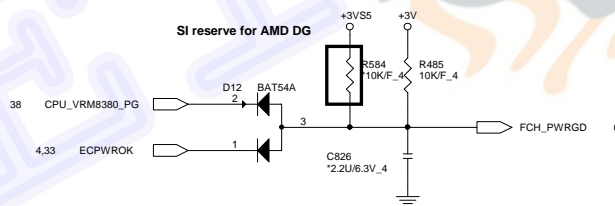
DEBUG STRAPS

FCH has 15K Internal Pull Up for PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIe STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIe STRAPS	ENABLE PCI MEM BOOT

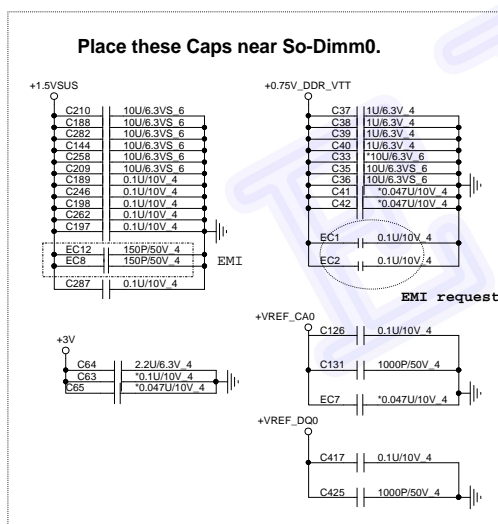
FCH PWRGD



PROJECT : R7X
Quanta Computer Inc.

Size Custom Document Number FCH 5/5(Strap &PWRGD)
Date: Tuesday, March 12, 2013 Sheet 10 of 43





SI change from short pad to *0R

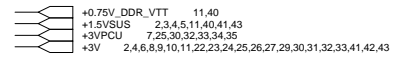
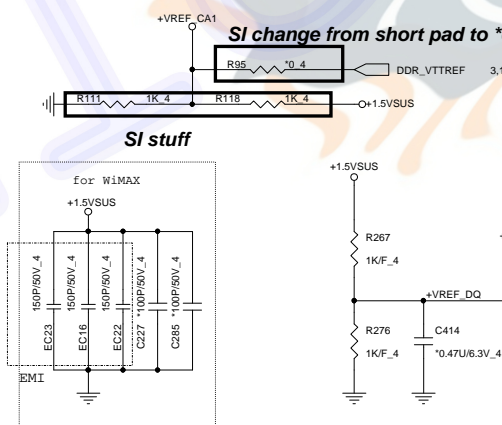
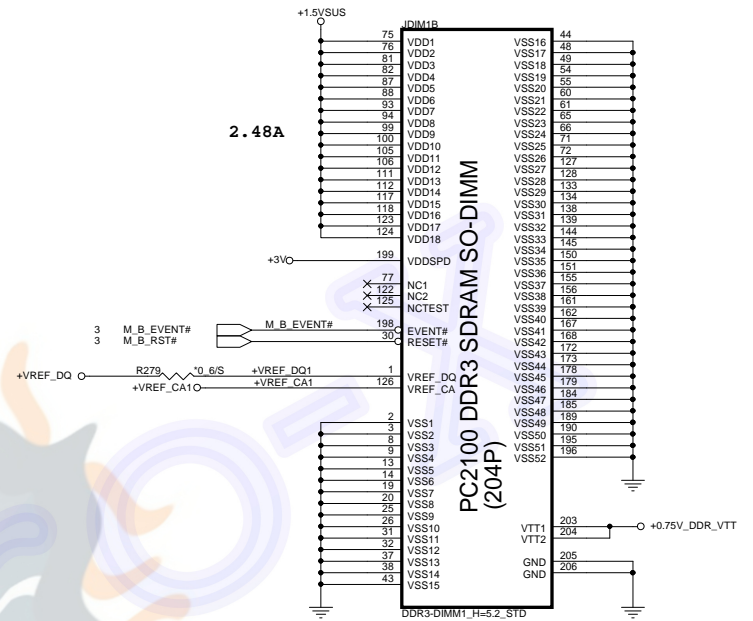
Diagram showing a signal path (SI stuff) connected to a source (+VREF_CAO) and a load (DDR_VTTREF). The path includes resistors R105 (1K_4) and R121 (1K_4). A resistor R93 (*0_4) is connected to the signal path, and the output is labeled 3.12,40. The signal path is also connected to a 1.5V source (+1.5VSUS).


- | | |
|----------------|---|
| +3V | 2,4,6,8,9,10,12,22,23,24,25,26,27,29,30,31,32,33,41,42,43 |
| +1.5V | 2,4,22,23,27,32,38,41 |
| +3VPCU | 7,25,30,32,33,34,35 |
| +1.5VSUS | 2,3,4,5,12,40,41,43 |
| +0.75V_DDR_VTT | 12,40 |

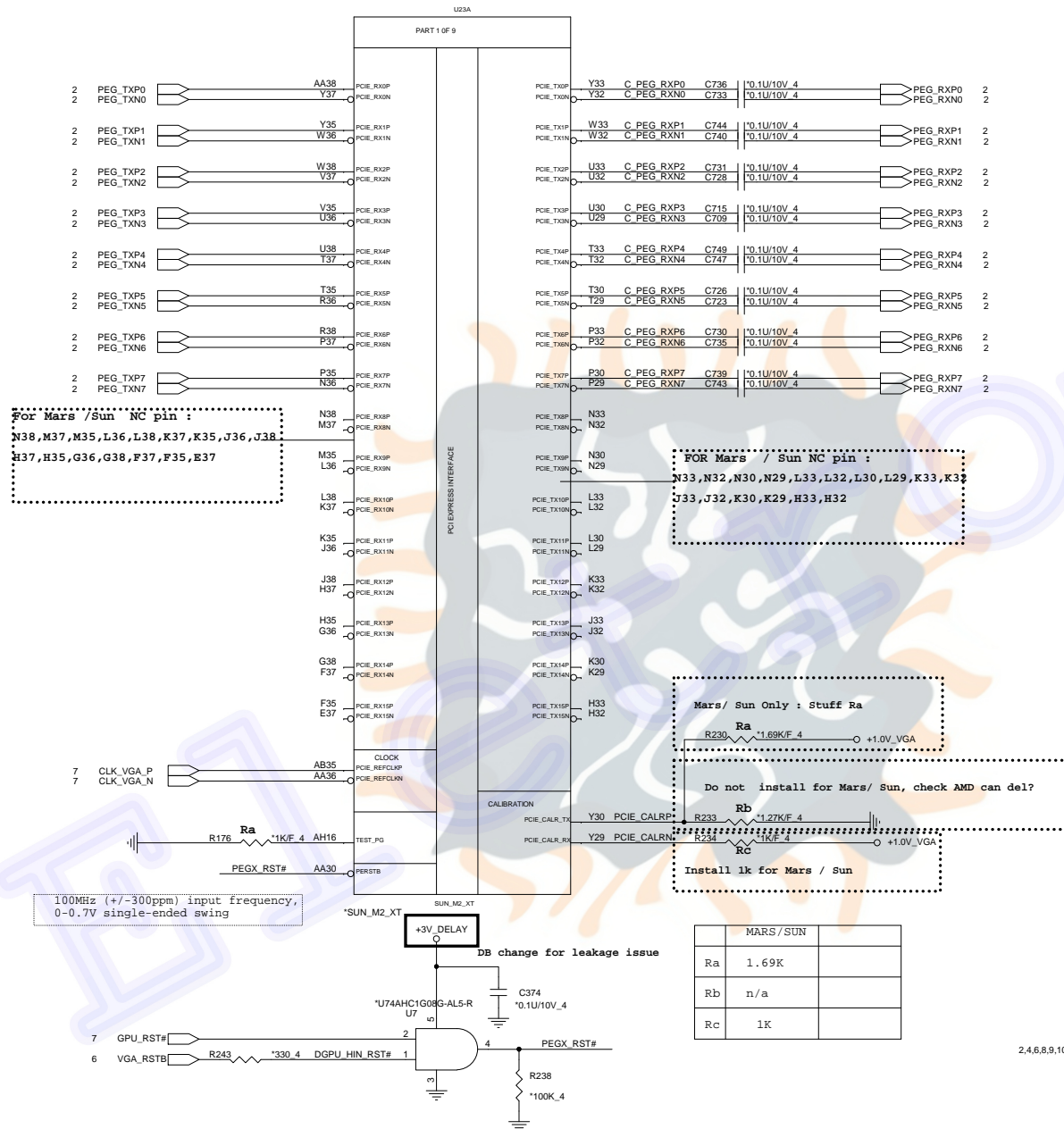


PROJECT : R7X
Quanta Computer Inc.

Size Custom	Document Number DDR3 DIMM0-STD (9.2H)
Date: Tuesday, March 12, 2013	Sheet




PROJECT : R7X
Quanta Computer Inc.
 Size Custom Document Number **DDR3 DIMM1-STD (5.2H)** Rev 1A
 Date: Tuesday, March 12, 2013 Sheet 1 of 1

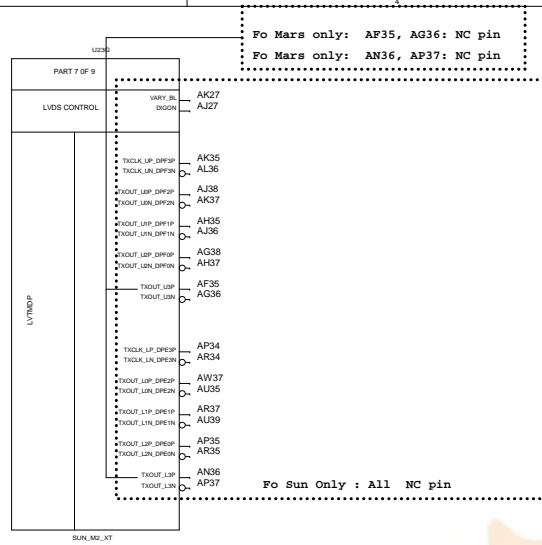


PROJECT : R7X
Qanta Computer Inc.

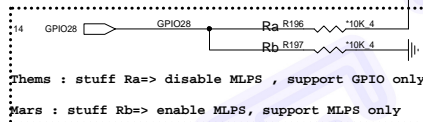
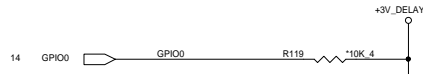
Size Custom Document Number SUN_PCIE_Interface Rev 1A
Date: Tuesday, March 12, 2013 Sheet 13



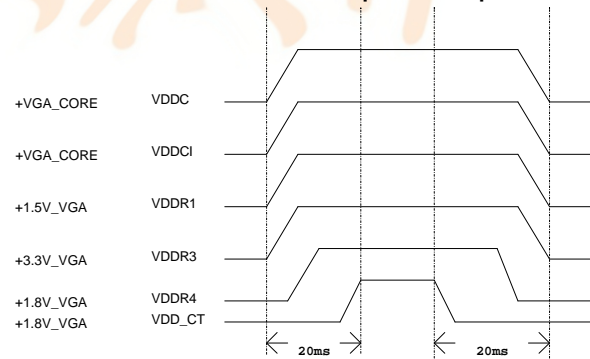




CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET				Default Setting
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	0
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	1
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIe Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	1
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIe Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA_DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512kbit M25P05A (STD) 101 - 1Mbit M25P10A (STD) 101 - 4Mbit M25P40 (STD) 101 - 512kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	001
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	0
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYN	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled Reserve for future ASIC	1
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	GENLK_CLK GPIO8 GPIO21 GENERICC	NOTE- ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOs ARE USED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	111



Power Up/Down Sequence




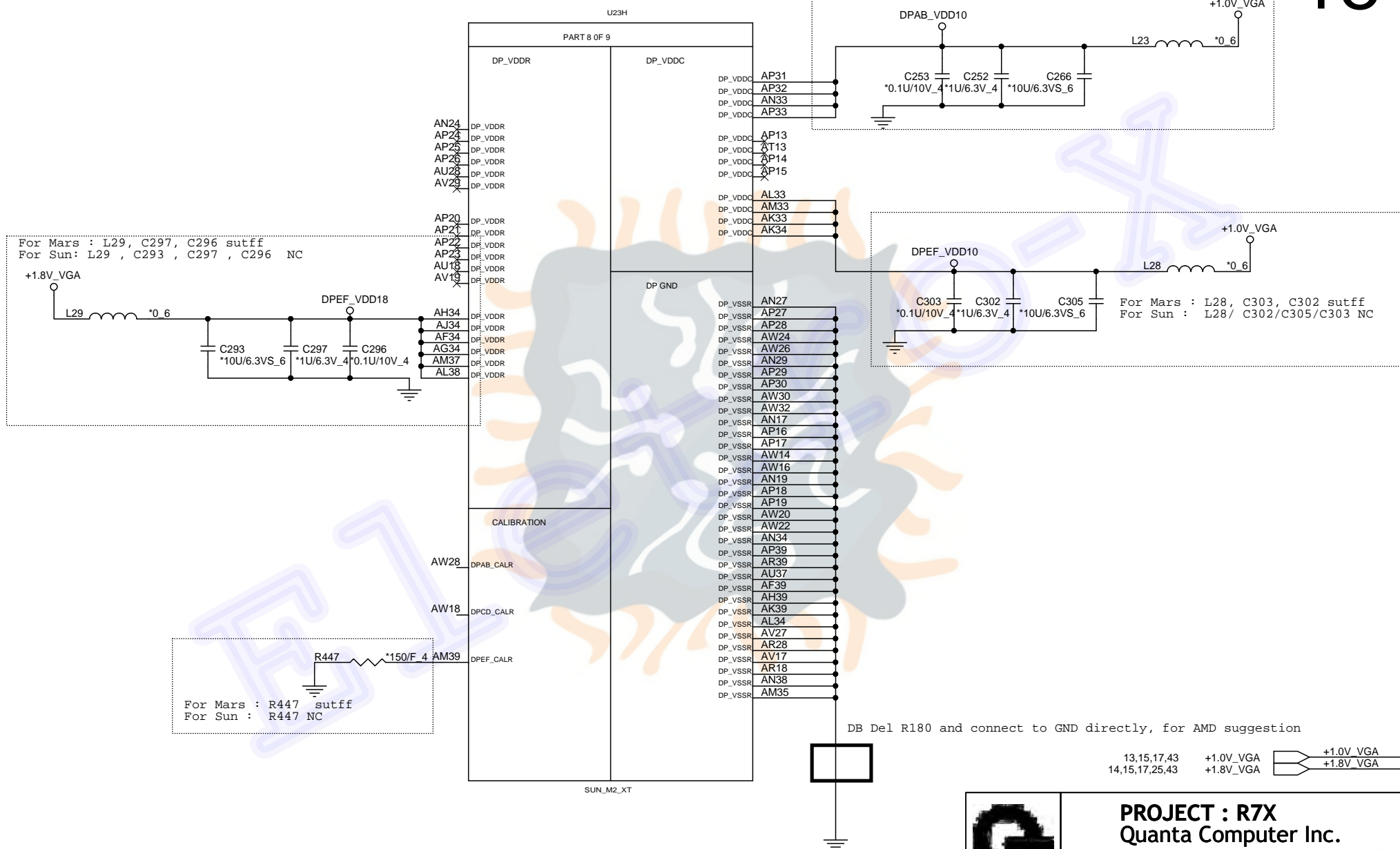


Note1. 1. No BACO Support :BIF_VDDC shorts with VDDC (Install Ra)

PX_EN = 0, for Normal Operation
PX_EN = 1, for BACO MODE

2. BACO Support: Refer to the BACO reference schematics/Application note for detail about BIF_VDDC Rail if BACO is Supported (Uninstall Ra)

 NB5	PROJECT : R7X Quanta Computer Inc.		
	Size Custom	Document Number SUN_Power & BACO	Revision 1
Date: Tuesday, March 12, 2013		Sheet 17 of 63	



NB5

PROJECT : R7X
Quanta Computer Inc.

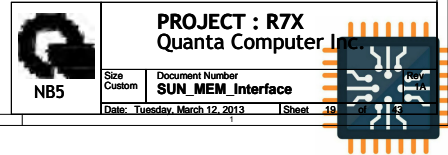
Size
Custom

Document Number
SUN_DP Powers

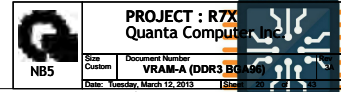
Date: Tuesday, March 12, 2013

Sheet 18 of

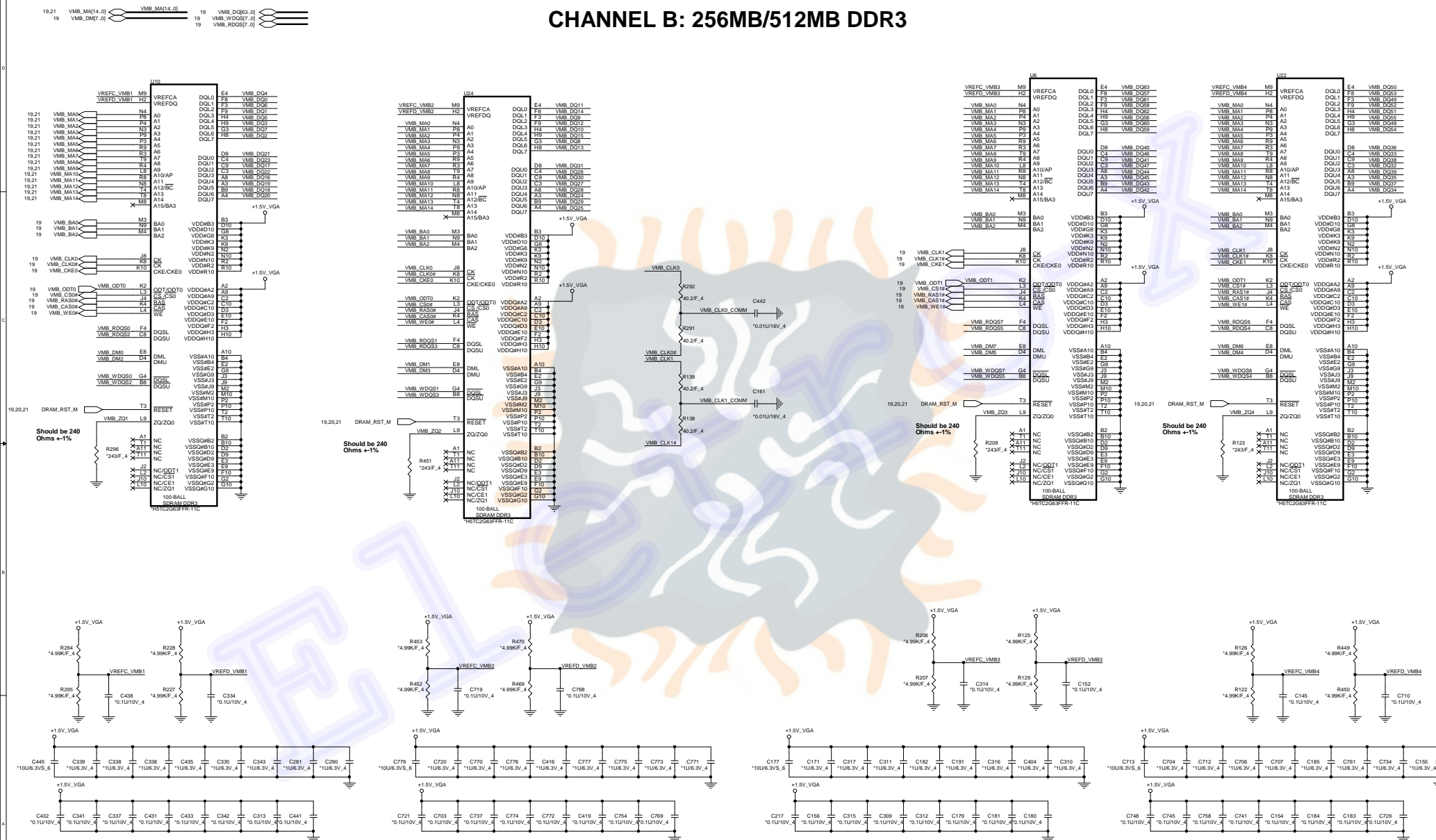




Eletro-X



CHANNEL B: 256MB/512MB DDR3



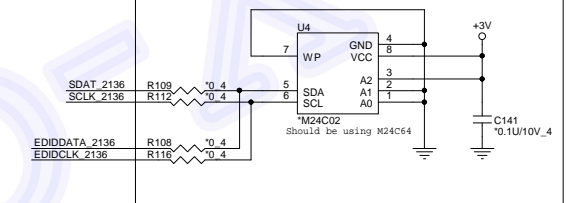
EDDID EEPROM
VCC

DP2LVDS VCC

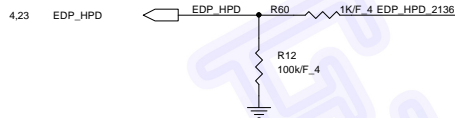
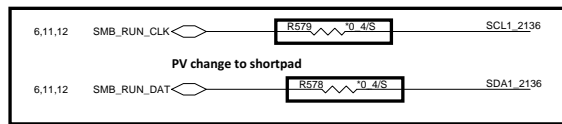
HPD

<=100ms

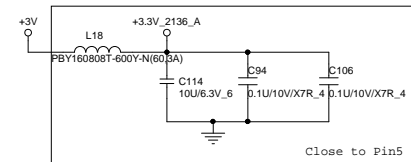
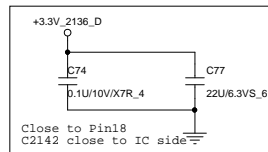
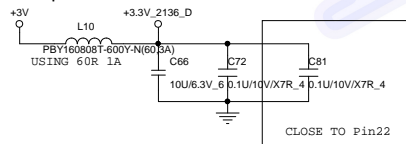
Reserve



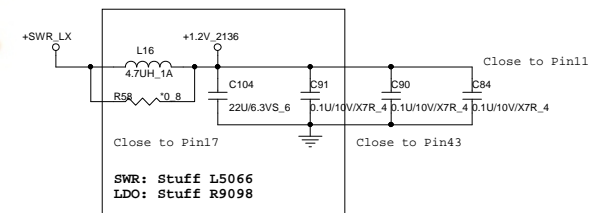
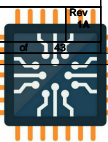
SMBUS



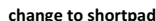
keep 80 Mile Trace



L69: need use CV-4709MN00 for Vendor suggestion

PROJECT : R7X
Quanta Computer Inc.Size
Custom Document Number
LVDS converter RTD2136
Date: Tuesday, March 12, 2013 Sheet 22 of 28

100

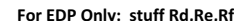
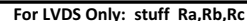


AL005243001 GMT:G5243AT11U
AL002821000 BCD:AP2821KTR-G1



Please note that 2011 camera is +3V a We do not need to use 5V -> 3.95V regulator

For EDP Only: stuff 0 Ohm



PROJECT RXX
Quanta Computer Inc

Si

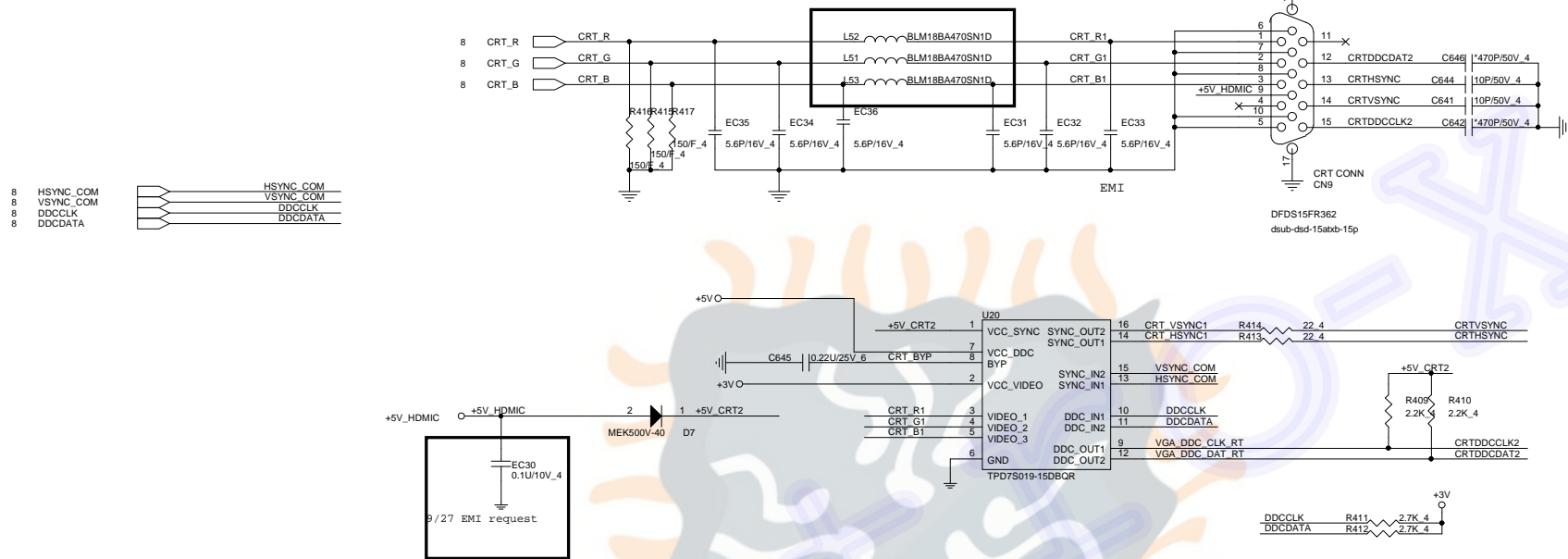
Document Number

Date: Tuesday, March 12, 2013 Sheet

Page 10 of 10

CRT PORT

SI change to 470Ω bead, BLM18BA470SN1D
for solve CRT rise/fall time issue



HOLE

HOLE

FAN hole

PCH BKT

CPU BKT

VGA BKT

Nut PN:MBBU2005010

THERMAL BKT

KB lock

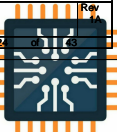
SI add

MV add

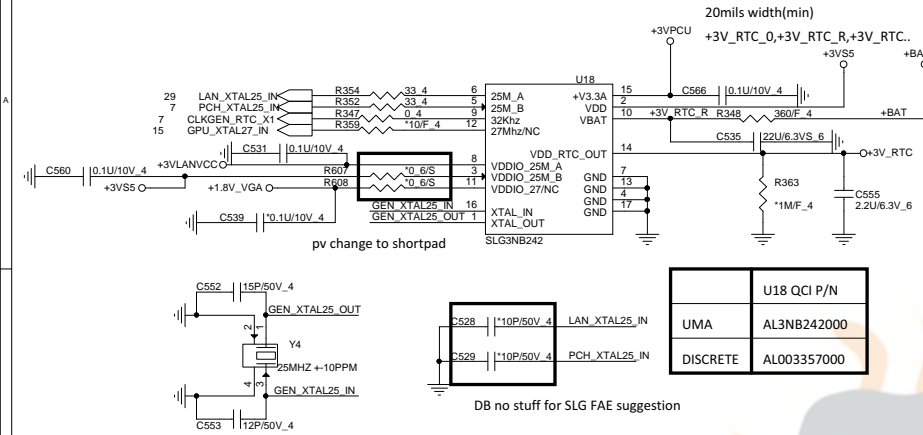


PROJECT : R7X
Quanta Computer Inc.

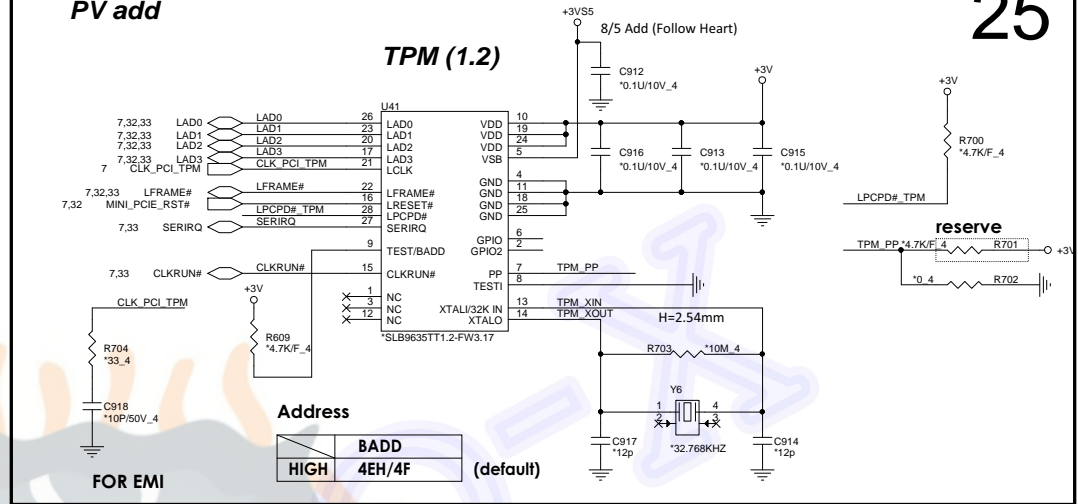
Size Custom Document Number
Date: Tuesday, March 12, 2013 Sheet 24



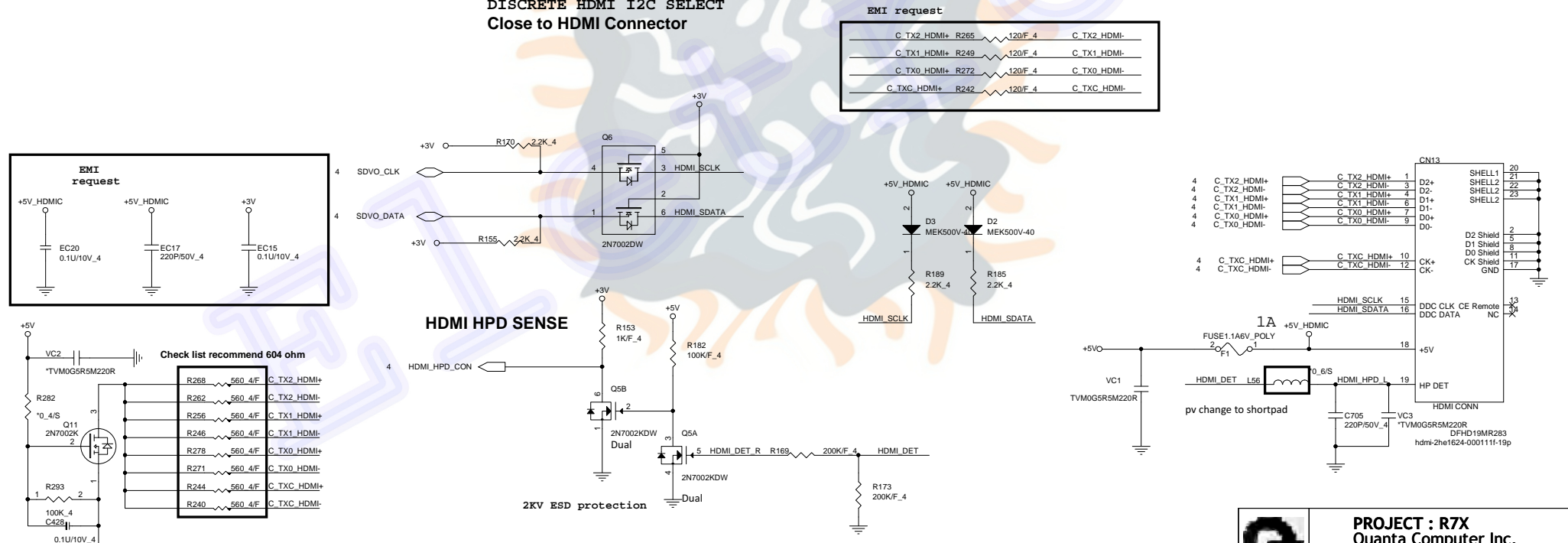
Green CLK Circuitry



PV add

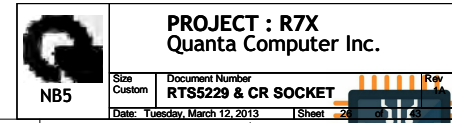


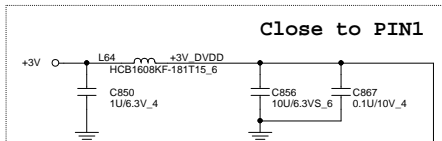
DISCRETE HDMI I2C SELECT Close to HDMI Connector



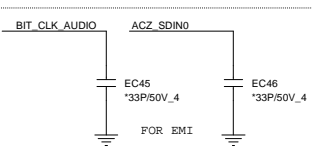
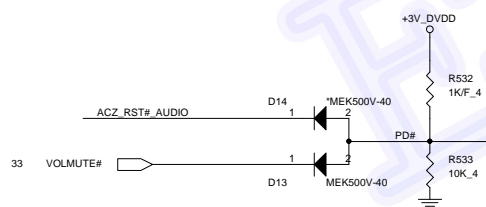
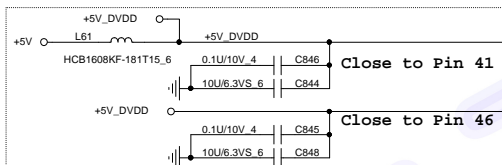
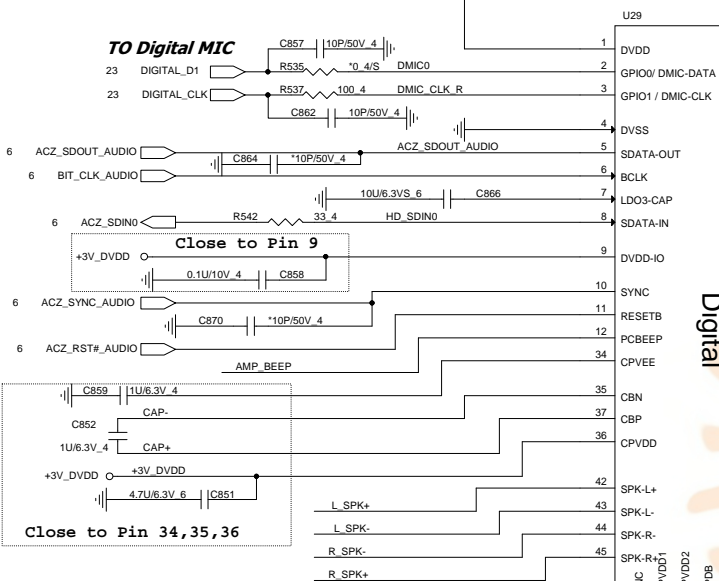
PROJECT : R7X
Quanta Computer Inc.

NB5
Size Custom
Document Number
HDMI
Date: Tuesday, March 12, 2013
Sheet 26

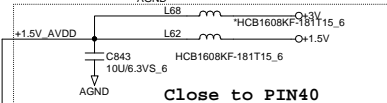
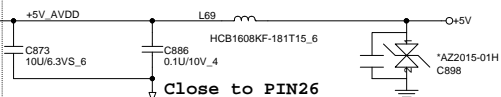




TO Digital MIC



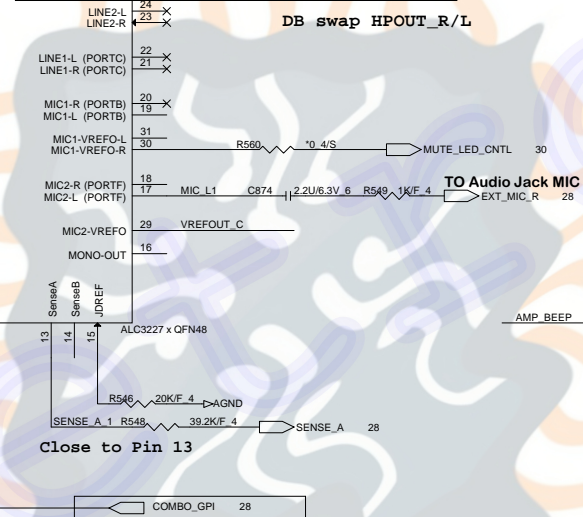
>40mils trace



Analog

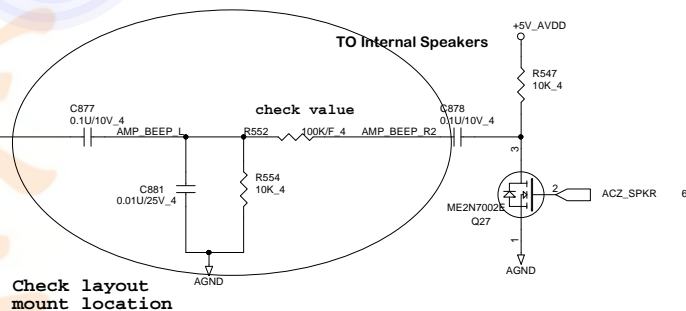
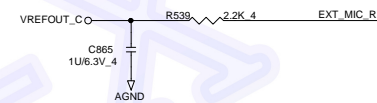
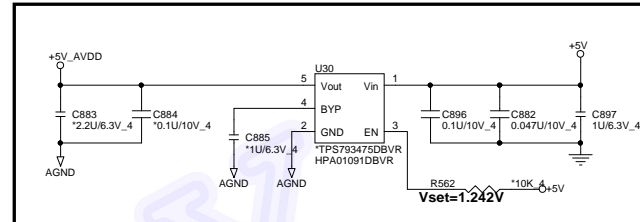


Digital



2,4,6,8,9,10,11,12,22,23,24,25,26,29,30,31,32,33,41,42,43
2,4,22,23,32,38,41

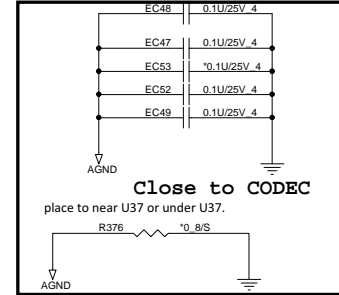
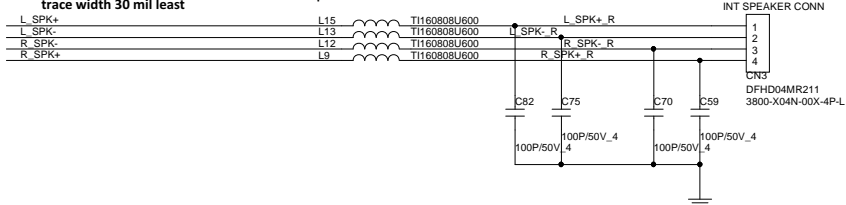
+5V
+3V
+1.5V



Check layout mount location

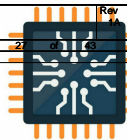
Keep L_SPK+/-, and R_SPK+/- trace width 30 mil least

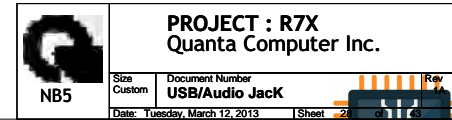
Close to CODEC
Speaker 4 ohm: 40mils

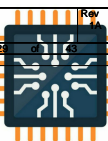
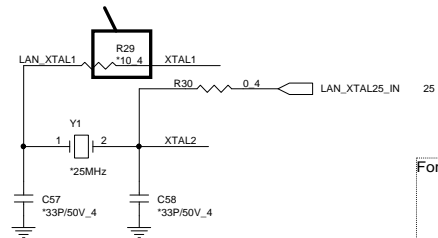


PROJECT : R7X
Quanta Computer Inc.

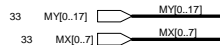
Size Custom Document Number **Azalia ALC3227**
Date: Tuesday, March 12, 2013 Sheet 2 of 43



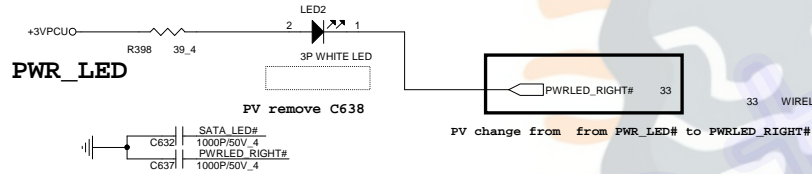
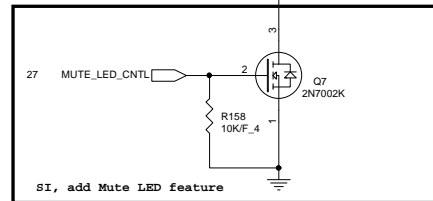
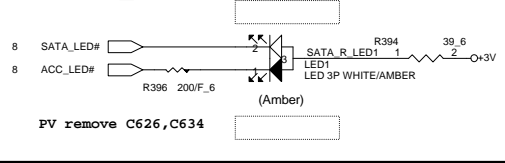




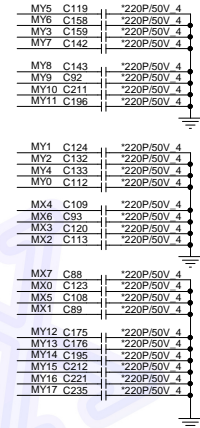
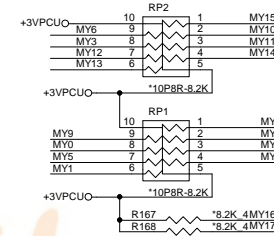
KEYBOARD Con.



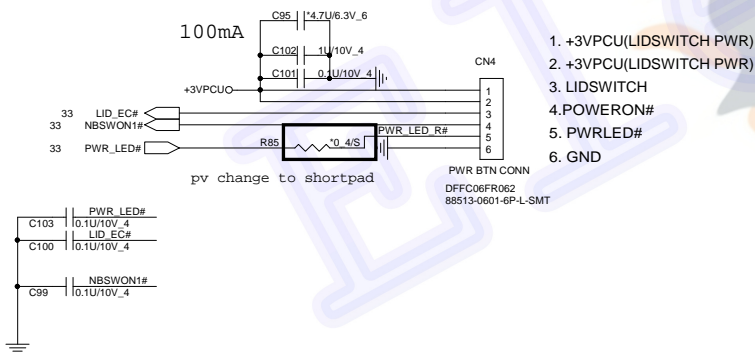
SATA_LED



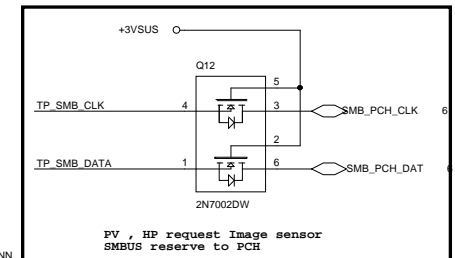
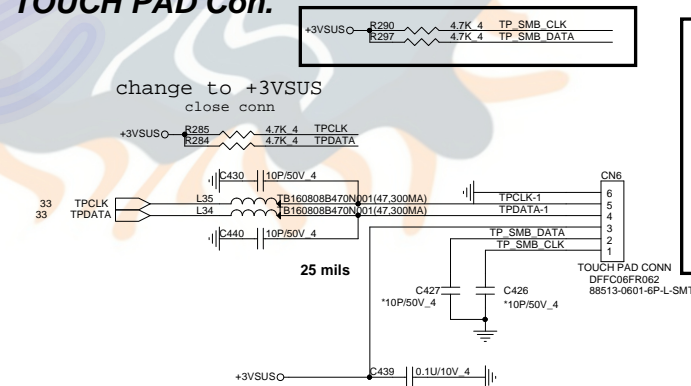
KEYBOARD PULL-UP



POWER BOTTON CONNECT



TOUCH PAD Con.

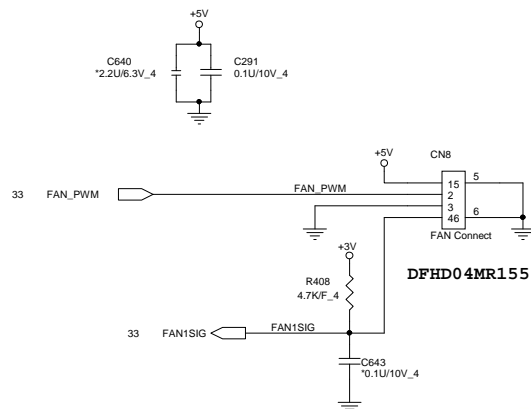


PROJECT : R7X
Quanta Computer Inc.

Size Custom Document Number LED/KB/SW/TP
Date: Tuesday, March 12, 2013 Sheet 30 of 43

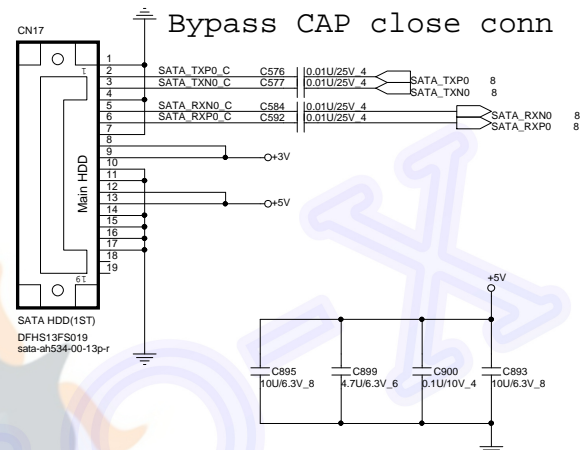


CPU FAN

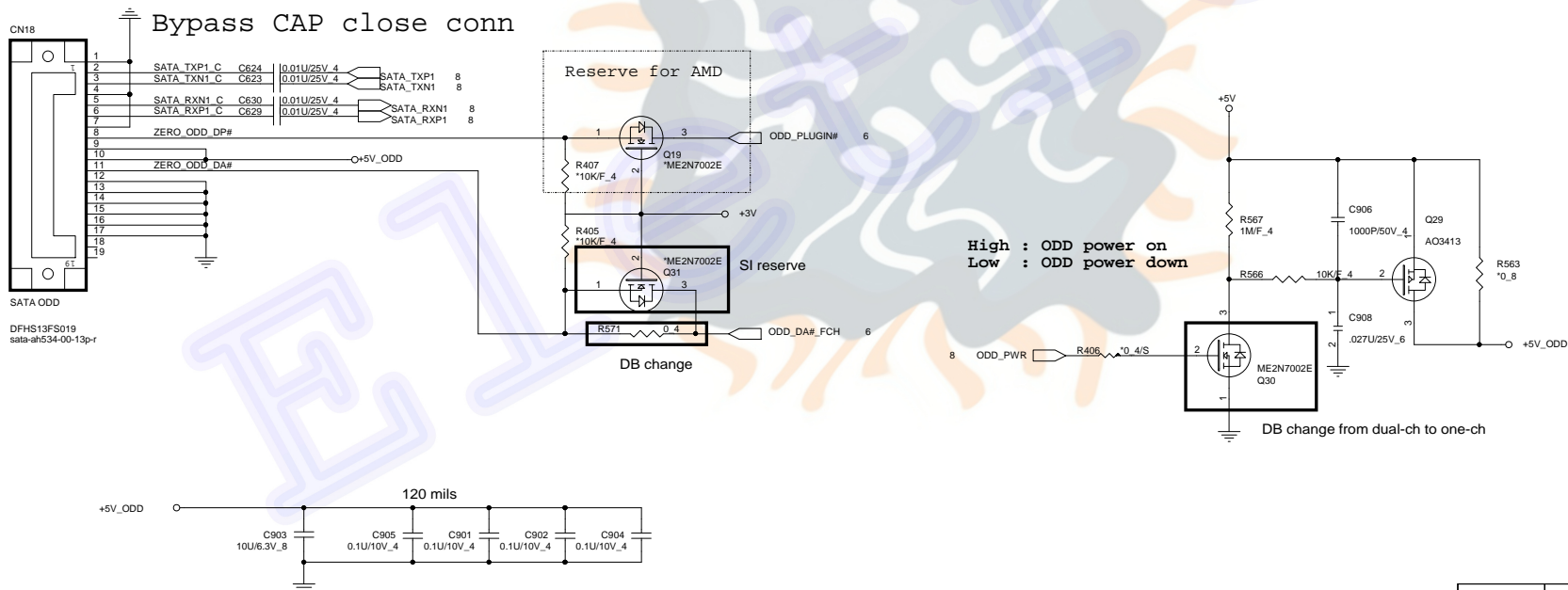



SATA HDD CONNECTOR

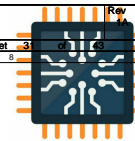
31



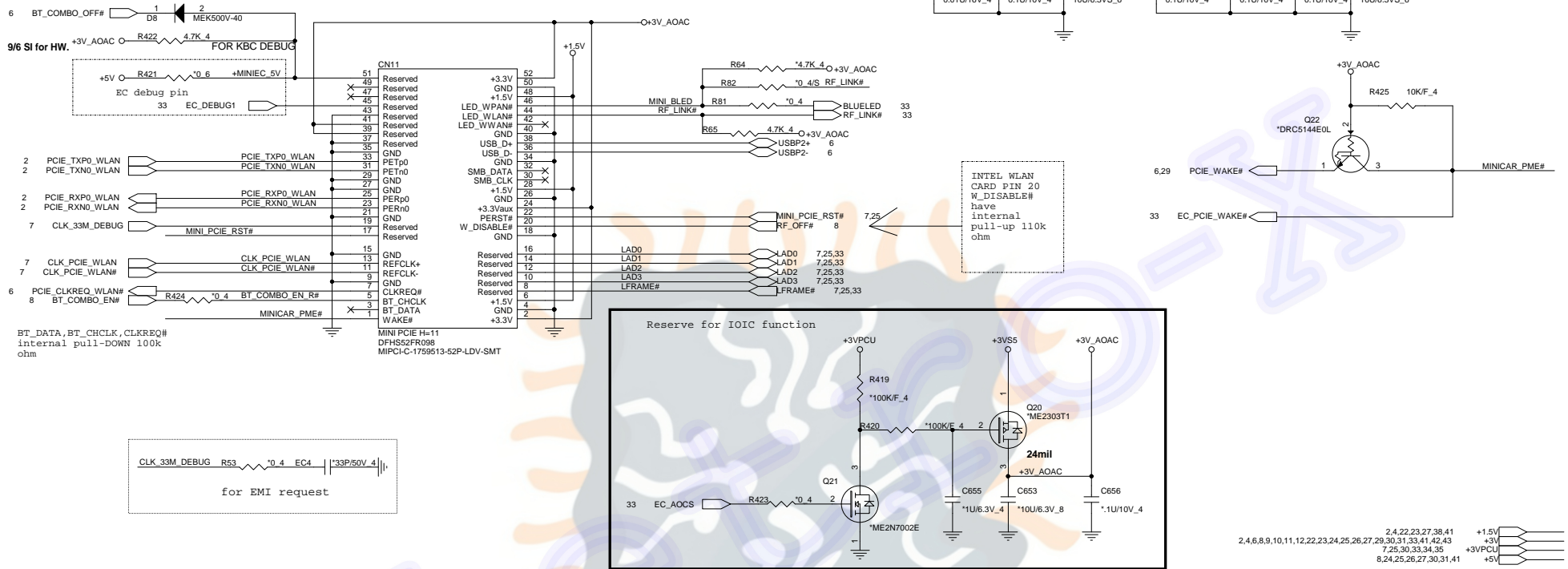
SATA ODD CONNECTOR



 NB5	PROJECT : R7X Quanta Computer Inc.	
	Size Custom	Document Number HDD/ODD/FAN
	Date: Tuesday, March 12, 2013	Sheet 3

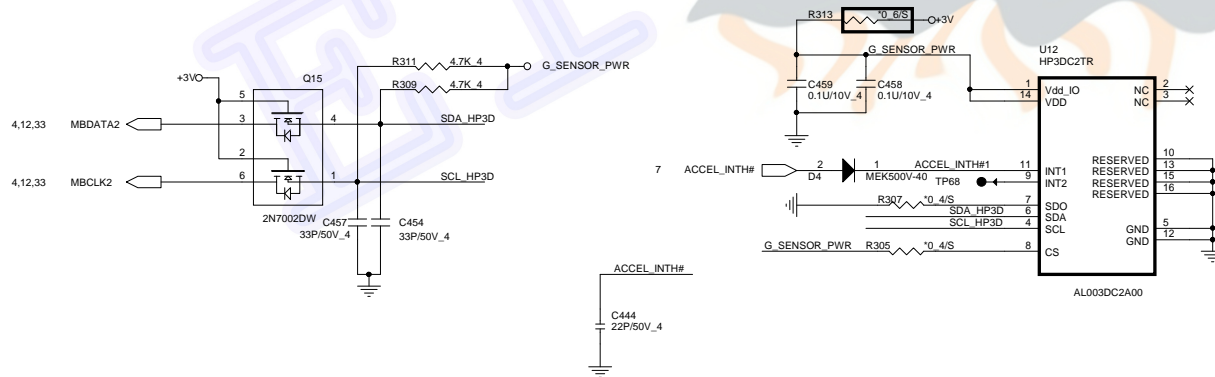


Mini PCI-E Card 1 WLAN



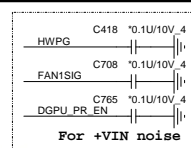
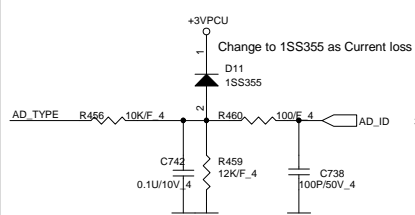
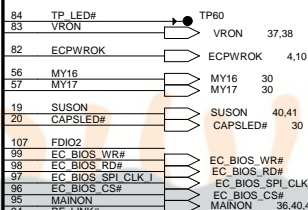
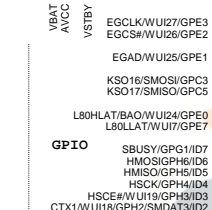
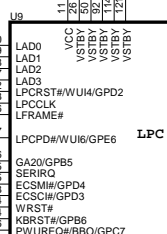
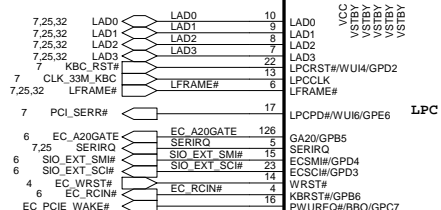
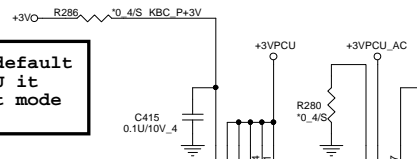
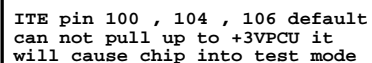
Accelerometer Sensor

PV change to shortpad

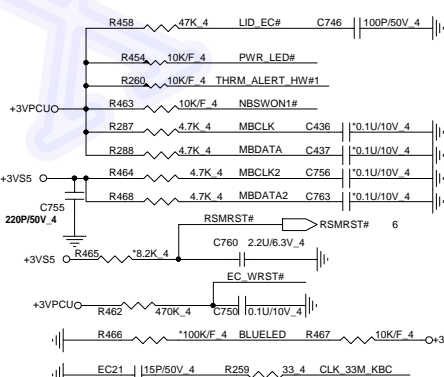
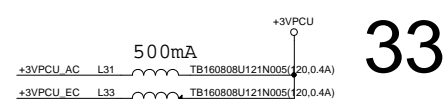


PROJECT : R7X
Quanta Computer Inc.

Size Custom	Document Number MINI PCIE CONN & G-sensor	Rev 1A
Date: Tuesday, March 12, 2013	Sheet 32	of 43

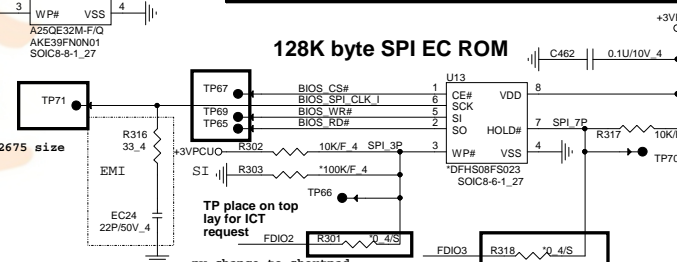


Vender	Size	P/N
AMIC	4M	AKE39ZN0800
EON	4M	AKE39ZN0Q03
WINBOND	4M	AKE39FN0N01
Socket		DFHS08FS023



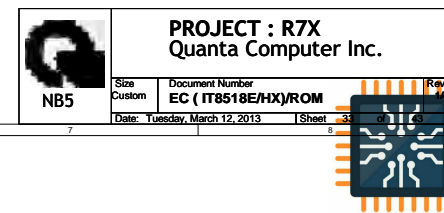
4M SPI EC ROM

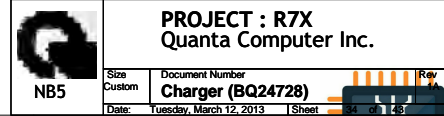
Signal	Pin	Internal Label	External Connection
BIOS CS#	1	CE#	VDD
BIOS SPI CLK I	6	SCK	
BIOS WR#	5	SI	
BIOS RD#	2	SO	HOLD#
SPI_3P	3	WP#	VSS
	8		+3VPC
	7		SPI_7P

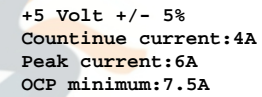
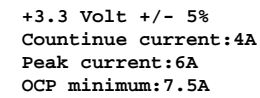


```
+3VPCUO---R232---10K/F 4 GPIO42 R218---10K/F 4---|
Hi ==> DIS/SG
Low ==>UMA
```

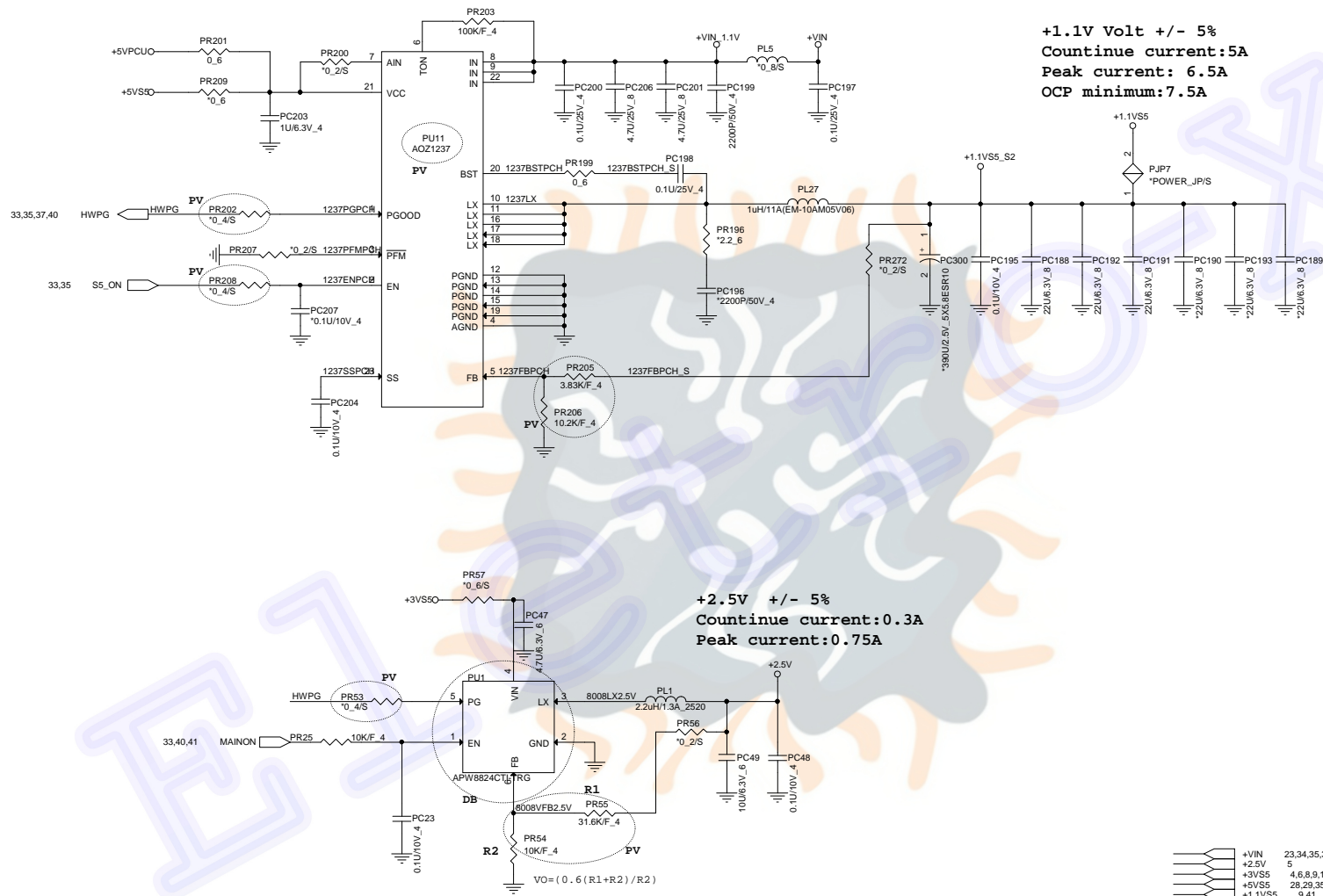
Platform model	GPIO42	adapte
SG/DIS	High	90W
UMA	Low	65W







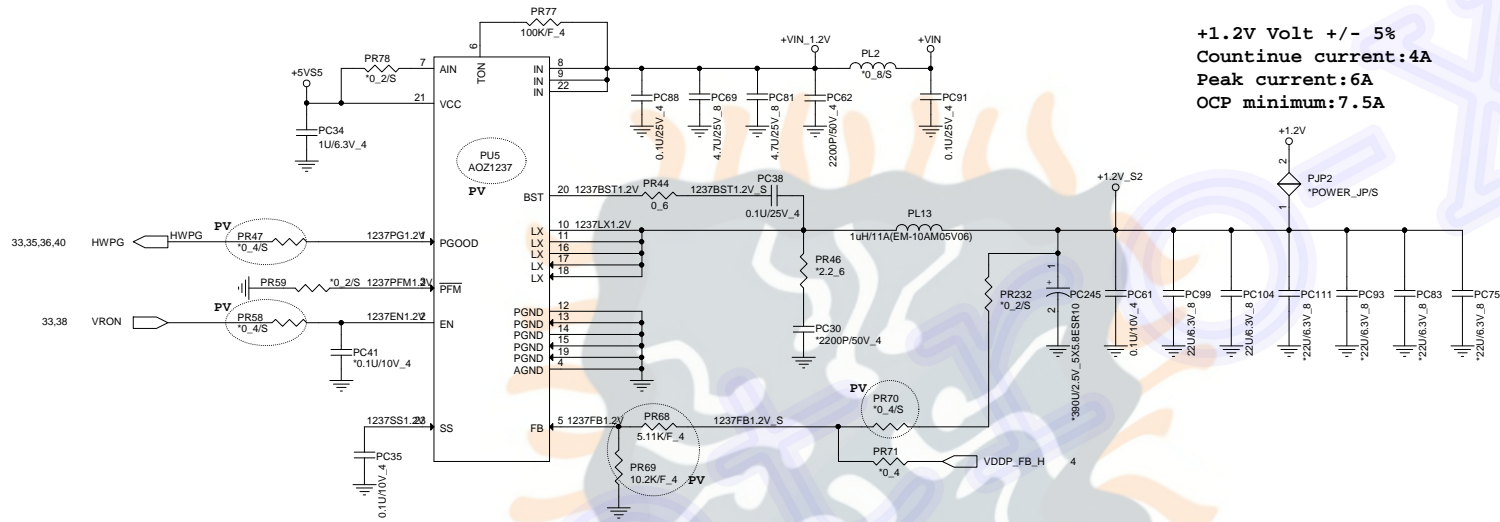
Size Custom	Document Number 3/5VS5 (NB670/NB671)	
Date:	Tuesday, March 12, 2013	Sheet



PROJECT : R7X
Quanta Computer Inc.

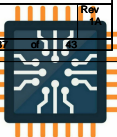
Size: Custom
 Document Number: **+1.1VS5 (AOZ1237)/2.5V**
 Date: Tuesday, March 12, 2013 Sheet 36

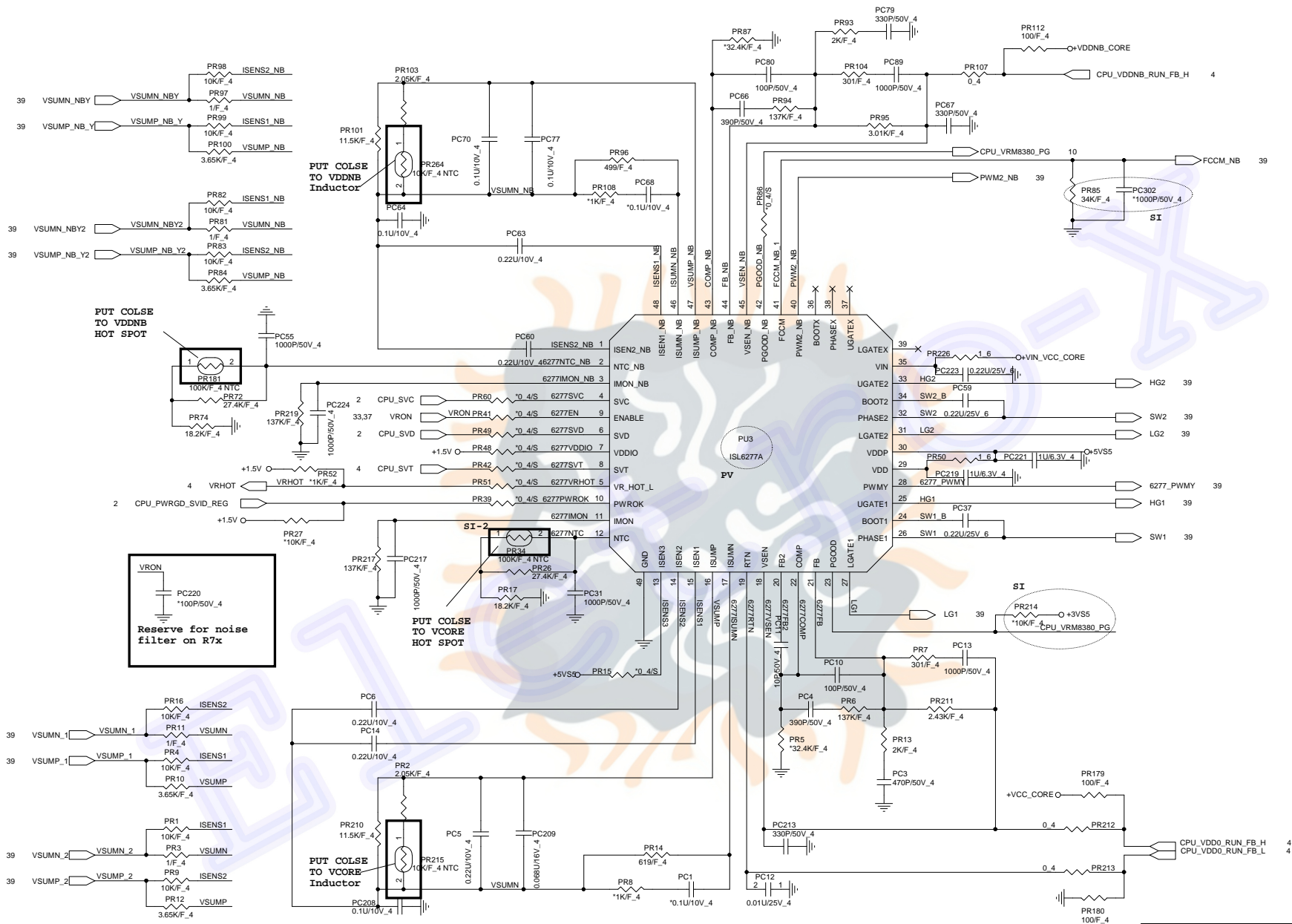


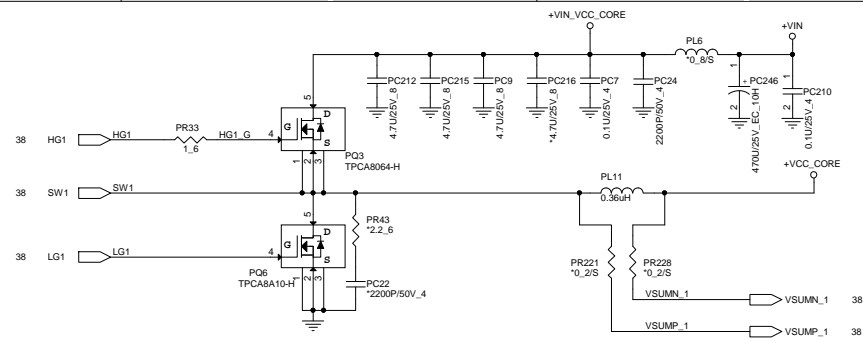


PROJECT : R7X
Quanta Computer Inc.

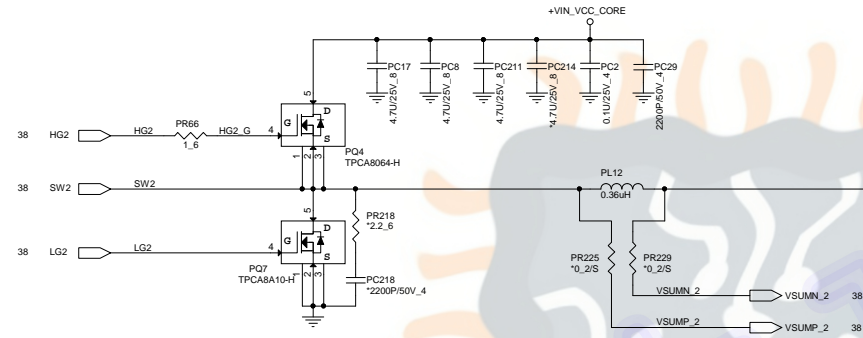
Size Custom	Document Number +1.2V (AOZ1237)	Rev 4
Date: Tuesday, March 12, 2013	Sheet 37	



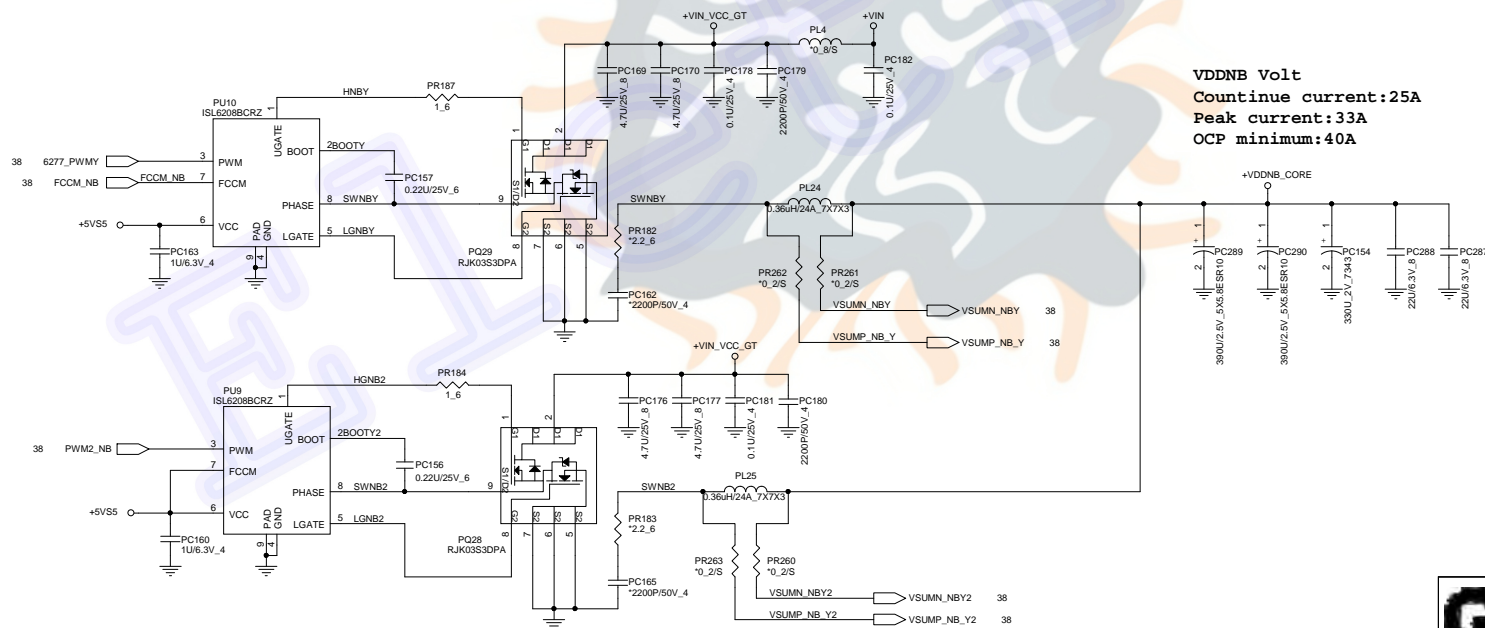





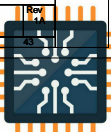
CPU CORE Volt
 Countinue current:36A
 Peak current:50A
 OCP minimum:60A

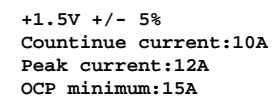


VDDNB Volt
 Countinue current:25A
 Peak current:33A
 OCP minimum:40A

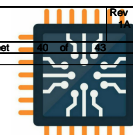


 NB5	PROJECT : R7X Quanta Computer Inc.	
	Size Custom	Document Number CPU Core2 (ISL6208)
	Date: Tuesday, March 12, 2013 Sheet 39 of 43	



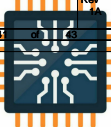


Size Custom	Document Number DDR3L(TPS51216)
Date:	Tuesday, March 12, 2013





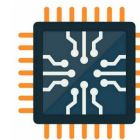
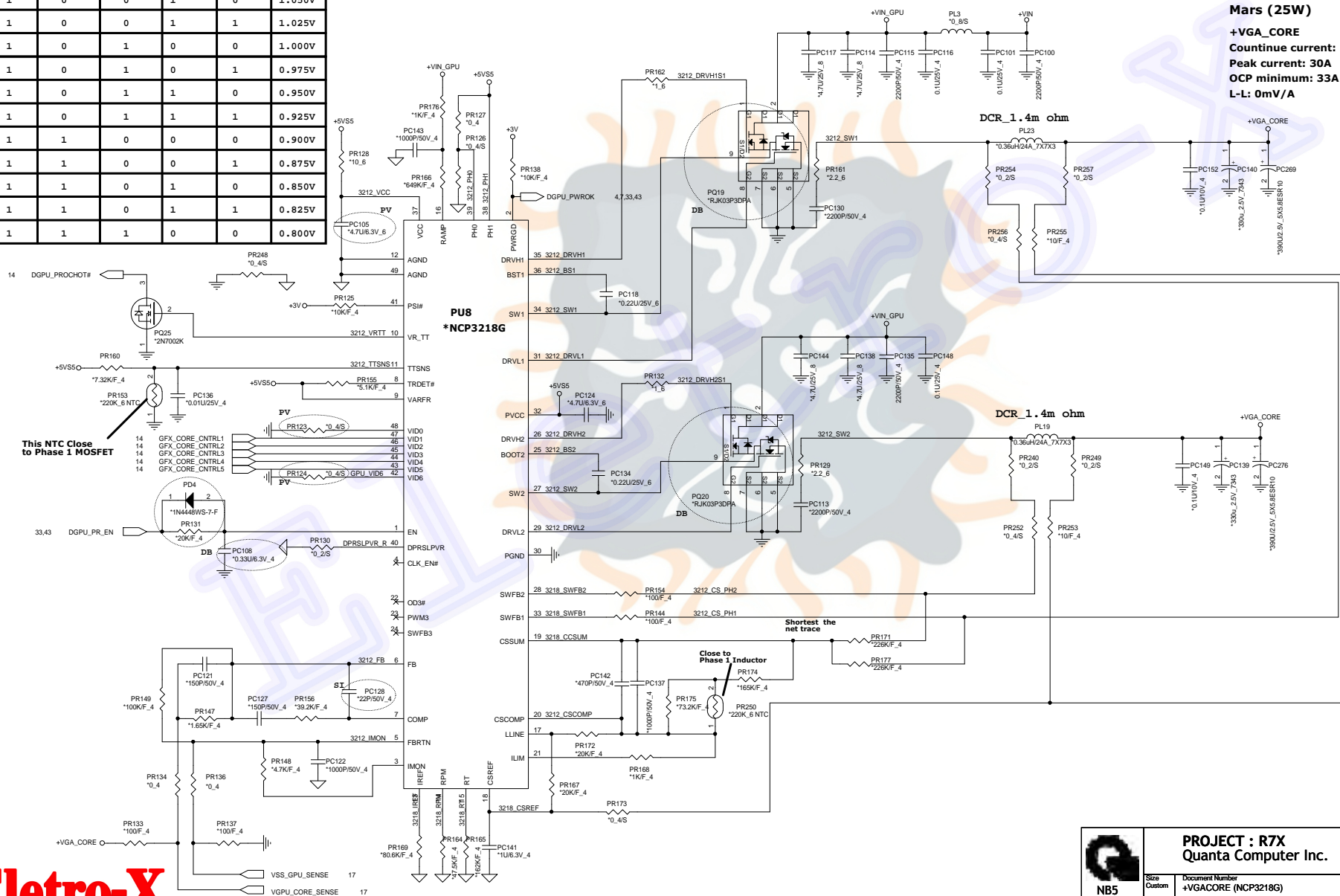
Size Custom	Document Number Dis-charge IC (SLG55448V)
Date: Tuesday, March 12, 2013	Sheet 4

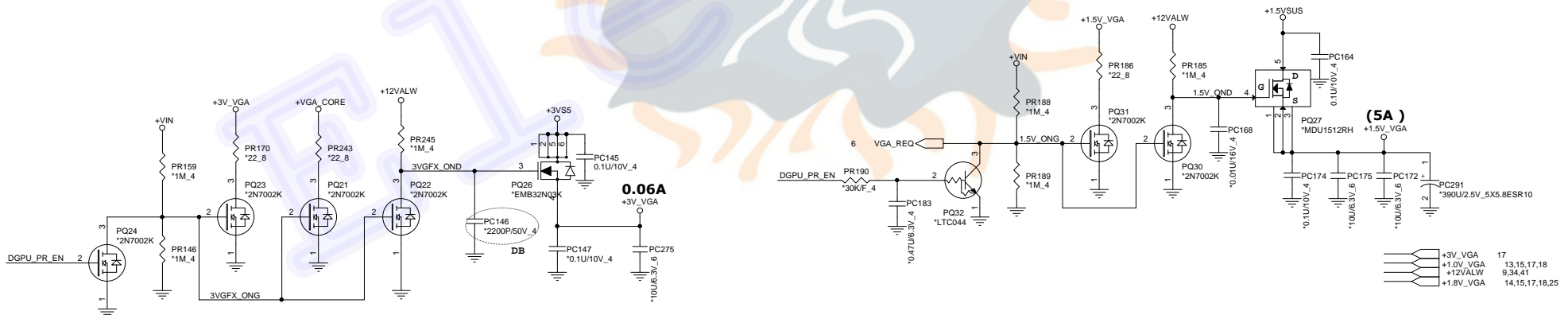
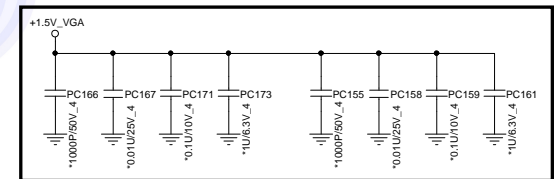
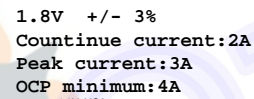
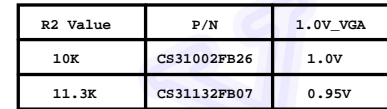


+VGA_CORE
Continue current: 25A
Peak current: 30A
OCP minimum: 33A
L-L: 0mV/A

PWRCNTL5	PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1	V-CORE
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V

Default





Size Custom	Document Number +1.0V_VGA/1.8V_VGA/3V_VGA	Rev 1A
Date: Tuesday, March 12, 2013	Sheet 43 of 43	